

CLAIMS

What is claimed is:

1. A line cache control system that controls data flow between a line cache, a first central processing unit (CPU) and first and second memory devices, comprising:

a first line cache interface that is associated with the first CPU, that receives a first program read request from the first CPU and that generates a first address from said first program read request;

a first memory interface that communicates with the first memory device;

a second memory interface that communicates with the second memory device;

a line cache; and

a switch that selectively connects said line cache to one of said first and second memory interfaces,

wherein when said line cache receives said first address, said line cache compares said first address to stored addresses in said line cache, returns data associated with said first address if a match occurs, and retrieves data from one of the first and second memory devices if a miss occurs.



2. The line cache control system of claim 1 wherein said first memory device is RAM.

3. The line cache control system of claim 2 wherein said RAM is one of DRAM, SDRAM, and DDRAM.

4. The line cache control system of claim 1 wherein said second memory device is flash memory.

5. The line cache control system of claim 1 wherein said first CPU is an advanced risc machine (ARM) processor.

6. The line cache control system of claim 1 further comprising:
a second CPU;
a second line cache interface that is associated with said second CPU, that receives a second program read request from said second CPU and that generates a second address from said second program read request; and
a line cache arbitration device that communicates with said first and second line cache interfaces and said line cache and that resolves line cache access conflicts between the first CPU and said second CPU.



7. The line cache control system of claim 6 further comprising:
 - a first direct interface that is associated with the first CPU,
 - wherein said first memory interface includes a second direct interface that communicates with said first direct interface and wherein said first and second direct interfaces allow the first CPU to at least one of read and write data directly to the first memory device.

8. The line cache control system of claim 7 further comprising:
 - a third direct interface that is associated with the second CPU,
 - wherein said second memory interface includes a fourth direct interface that communicates with said third direct interface and wherein said third and fourth direct interfaces allow said second CPU to at least one of read and write data directly to the second memory device.

9. The line cache control system of claim 8 further comprising a direct read/write arbitration device that resolves direct memory access conflicts between said first and third direct interfaces.



10. The line cache control system of claim 6 wherein the first CPU is a host processor for a hard disk drive and said second CPU is a servo processor for said hard disk drive.

11. The line cache control system of claim 1 wherein said line cache includes:

line cache memory that stores data;
a content addressable memory (CAM) that stores addresses associated with said data stored in said line cache memory; and
a line cache module that includes a line cache state machine that determines when one of a hit and a miss occurs and that manages retrieval of data from the first and second memory devices when said miss occurs.

12. The line cache control system of claim 11 wherein said line cache memory includes multiple pages and wherein said line cache module allows one page to be accessed by one of the first CPU and said second CPU while the other of the first CPU and said second CPU is waiting for data retrieval in another page.

13. The line cache control system of claim 11 further comprising a least used page device that identifies a least used page in said line cache.



14. The line cache control system of claim 13 wherein said least used page device replaces said least used page with data retrieved from one of the first and second memory devices when a miss occurs.

15. The line cache control system of claim 11 wherein state transitions of said line cache state machine are based, in part, on at least one internal state of the CPU.

16. The line cache control system of claim 14 wherein said least used page device identifies a second least used page and wherein said line cache state module checks internal states of the CPU.

17. The line cache control system of claim 16 wherein said least used page is replaced when a miss occurs and internal states of the CPU do not indicate a likelihood that said least used page will be needed within a predetermined period.

18. The line cache control system of claim 17 wherein said second least used page is replaced when a miss occurs and internal states of the CPU indicate a likelihood that said least used page will be needed within a predetermined period.



19. The line cache control system of claim 1 wherein said CPU executes an application and wherein said line cache has a line width and number of pages that are based on said application.

20. The line cache control system of claim 1 wherein said line cache includes 4 pages of 8 x 32.

